**Question Bank**

Subject: Digital Electronics / Digital System Design

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|  | Convert the decimal number 673.23 to binary |  |
|  | Find the 9’s complement of the decimal number 12349876. |  |
|  | Discuss how XOR gate can be used as an inverter. |  |
|  | Prove that the function F= AB + BC + CA is a dual of itself. |  |
|  | In the following perform the indicated operation without converting to decimal:1. (367)8 + (715)8
2. (12B)16 - (A7)16
 |  |
|  | Express the following function into both the canonical forms: F = ABC + A’B + BC’ |  |
|  | Design a full subtractor and implement it using only NAND gates. |  |
|  | Reduce the following Boolean expressions to the indicated number of literals:(a) *A’C’+ ABC + AC’* to three literals(b) *(x’ y’ + z)’ + z + xy + wz* to three literals(c) *A’ B (D’ + C’ D ) + B (A + A’ CD)* to one literals(d) *( A’ + C)(A’ + C’)(A + B + C’D)* to four literals |  |
|  | Find the complement of *F = x + yz*; then show that *F . F’ =* oand  *F + F’ = 1*. |  |
|  | Find the complement of the following expression:1. *xy’ + x’ y*
2. *(AB’ + C)D’ + E*
3. *AB(C’ D’ +CD’) +A’ B(C’ + D)(C + D’)*
 |  |
|  | Obtain the truth table of the following function and express each function in sum of minterms and product of maxterms:1. *(xy + z)(y + xz)*
2. *(A’ + B)(B’ + C)*
3. *y’z + wxy’ + wxz’ + w’ x’ z*
 |  |
|  | Express the following function in sum of miniterms and product of maxterms:1. *F (A, B, C, D) = B’ D + A’ D +BD*
2. *F(x, y, z) = (xy + z)(xz + y)*
 |  |
|  | Convert the following to the other canonical from:1. $F(x,y,z) = \sum\_{}^{}(1,3,7)$
2. (b) $F(A,B,C,D) = \prod\_{}^{}(0,1,2,3,4,6,12)$
 |  |
|  | Simplify the following Boolean function F together with the don’t-care conditions d: F(A,B,C,D) = ∑(3,4,13,15); d(A,B,C,D) = ∑( 1,2,5,6,8,10,12,14) |  |
|  | Design a full subtractor and implement it using only (i) NAND gates (ii) NOR gates |  |
|  | Design a full adder and implement it using two multiplexers. |  |
|  | Design a 5-line to 32-line decoder using 3-line to 8-line decoders. |  |
|  | Four inputs – A,B,C,D – are to be observed to generate an output, Z. The output Z should be high only when exactly two of the inputs are high or when all the inputs are high. 1. Write a truth table for this function
2. Implement this function using only one 8:1 MUX.
3. Find a minimal expression for this function using the QM method.
4. Find a minimal expression for this function using K-map.
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|  | Design a BCD to excess-3 code converter using NAND gates only. |  |
|  | Find a minimal expression for the function *F* using K-map*F* = ∑(1,3,4,6,7,12,15,19,24,25,29,32) |  |
|  | Design a full adder and implement it using two multiplexers. |  |
|  | Design a 5-line to 32-line decoder using 3-line to 8-line decoders. |  |
|  | What is the difference between a latch and a flip-flop |  |
|  | Differentiate between positive edge triggered and negative edge triggered devices. |  |
|  | Modify a JK flip flop to work as:1. A D flip flop
2. A T flip flop
 |  |
|  | Write a note on Universal shift register. |  |
|  | (a) What is a race around condition in flip flops? |  |
|  | (b) Explain the working of a Master-Slave JK flip flop. Also explain how it helps to resolve the problem of race-around. |  |
|  | Design a counter using T flip flops to count the sequence 0,2,4,6,7,9,11,13 and back to zero. Your design should avoid lock out condition. |  |
|  | Design a ring counter using 4 flip flops. |  |
|  | What is a Johnson or Twisted Ring Counter? Design a twisted ring counter using 3 flip flops |  |