# **Electronics Tutorial Series** DIODES

#### **The PN Junction**

#### Steady State<sup>1</sup>



#### **The PN Junction**



#### **Steady State**

When no external source is connected to the pn junction, diffusion and drift balance each other out for both the holes and electrons

**Space Charge Region:** Also called the depletion region. This region includes the net positively and negatively charged regions. The space charge region does not have any free carriers. The width of the space charge region is denoted by W in pn junction formula's.

**Metallurgical Junction:** The interface where the p- and n-type materials meet.

**<u>Na & Nd:</u>** Represent the amount of negative and positive doping in number of carriers per centimeter cubed. Usually in the range of 10<sup>15</sup> to 10<sup>20</sup>.

#### **The Biased PN Junction**



The pn junction is considered biased when an external voltage is applied. There are two types of biasing: Forward bias and Reverse bias. These are described on then next slide.

#### **The Biased PN Junction**

#### Forward Bias:



In forward bias the depletion region shrinks slightly in width. With this shrinking the energy required for charge carriers to cross the depletion region decreases exponentially. Therefore, as the applied voltage increases, current starts to flow across the junction. The barrier potential of the diode is the voltage at which appreciable current starts to flow through the diode. The barrier potential varies for different materials.





Under reverse bias the depletion region widens. This causes the electric field produced by the ions to cancel out the applied reverse bias voltage. A small leakage current, Is (saturation current) flows under reverse bias conditions. This saturation current is made up of electron-hole pairs being produced in the depletion region. Saturation current is sometimes referred to as scale current because of it's relationship to junction temperature.

#### **Properties of Diodes**

Figure 1.10 – The Diode Transconductance Curve<sup>2</sup>



- V<sub>D</sub> = Bias Voltage
- I<sub>D</sub> = Current through Diode. I<sub>D</sub> is Negative for Reverse Bias and Positive for Forward Bias
- I<sub>s</sub> = Saturation
  Current
- V<sub>BR</sub> = Breakdown
  Voltage
- V<sub>\u03c6</sub> = Barrier Potential Voltage

#### The Q Point

The operating point or Q point of the diode is the quiescent or nosignal condition. The Q point is obtained graphically and is really only needed when the applied voltage is very close to the diode's barrier potential voltage. The example <sup>3</sup> below that is continued on the next slide, shows how the Q point is determined using the transconductance curve and the load line.

 $R_{S} = 1000 \Omega$   $V_{A} = 6V - V_{\phi}$ 

First the load line is found by substituting in different values of  $V_{\phi}$  into the equation for  $I_D$  using the ideal diode with barrier potential model for the diode. With  $R_S$  at 1000 ohms the value of  $R_F$  wouldn't have much impact on the results.

$$I_{\rm D} = \frac{V_{\rm A} - V_{\phi}}{R_{\rm S}}$$

Using V  $_{\phi}$  values of 0 volts and 1.4 volts we obtain I<sub>D</sub> values of 6 mA and 4.6 mA respectively. Next we will draw the line connecting these two points on the graph with the transconductance curve. This line is the load line.

#### The Q Point



#### **Dynamic Resistance**

The dynamic resistance of the diode is mathematically determined as the inverse of the slope of the transconductance curve. Therefore, the equation for dynamic resistance is:



The dynamic resistance is used in determining the voltage drop across the diode in the situation where a voltage source is supplying a sinusoidal signal with a dc offset.

The ac component of the diode voltage is found using the following equation:

$$v_F = v_{ac} \frac{r_F}{r_F + R_S}$$

The voltage drop through the diode is a combination of the ac and dc components and is equal to:

 $V_D = V_{\phi} + v_F$ 

#### **Types of Diodes and Their Uses**

#### PN Junction Diodes:

Are used to allow current to flow in one direction while blocking current flow in the opposite direction. The pn junction diode is the typical diode that has been used in the previous circuits.

Schematic Symbol for a PN Junction Diode



Representative Structure for a PN Junction Diode



Are specifically designed to operate under reverse breakdown conditions. These diodes have a very accurate and specific reverse breakdown voltage.



Schematic Symbol for a Zener Diode

### **Tubes, Transistors and Amplifiers**



### **Bipolar Transistor Construction**

• NPN / PNP Block Diagrams



# **Bipolar Transistor Theory**

- For *any* transistor to conduct, two things must occur.
  - The emitter base PN junction <u>must</u> be forward biased.
  - The base collector PN junction <u>must</u> be reverse biased.

# **Bipolar Transistor Biasing (NPN)**



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# **Bipolar Transistor Operation (PNP)**

•90% of the current carriers pass through the reverse biased base - collector PN junction and enter the collector of the transistor.

•10% of the current carriers exit transistor through the base.

•The opposite is true for a NPN transistor.

# **Amplifier Operation**

- The transistor below is biased such that there is a degree of forward bias on the base emitter PN junction.
- Any input received will change the magnitude of forward bias & the amount of current flow through the transistor.



### **Amplifier Electric Switch Operation**

•When the input signal is large enough, the transistor can be driven into saturation & cutoff which will make the transistor act as an electronic switch.

•Saturation - The region of transistor operation where a further increase in the input signal causes no further increase in the output signal.

•*Cutoff* - Region of transistor operation where the input signal is reduced to a point where minimum transistor biasing cannot be maintained => the transistor is no longer biased to conduct. (no current flows)

### **Amplifier Electric Switch Operation**

#### -Transistor Q-point

•*Quiescent point* : region of transistor operation where the biasing on the transistor causes operation / output with no input signal applied.

-The biasing on the transistor determines the amount of time an output signal is developed.

#### -Transistor Characteristic Curve

•This curve displays all values of  $I_C$  and  $V_{CE}$  for a given circuit. It is curve is based on the level of DC biasing that is provided to the transistor prior to the application of an input signal.

–The values of the circuit resistors, and  $\mathbf{V}_{CC}$  will determine the location of the Q-point.

#### **Transistor Characteristic Curve**



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#### **Common Emitter Schematic**



### **Kirchoff Voltage Law**

 DC Kirchoff Voltage Law Equations and Paths +V<sub>CC</sub>



**Base - Emitter Circuit**   $I_BR_B + V_{BE} - V_{CC} = 0$  **Collector - Emitter Circuit**  $I_CR_C + V_{CE} - V_{CC} = 0$ 

#### **Common Base Schematic**



### **Kirchoff Voltage Law**

• DC Kirchoff Voltage Law Equations and Paths



### **Common Base Operation**



#### **Positive Going Signal**

Base becomes more (+) WRT Emitter  $\Rightarrow$  FB  $\downarrow \Rightarrow$   $I_C \downarrow \Rightarrow$   $V_{R_C} \downarrow \Rightarrow$   $V_C \uparrow \Rightarrow$  $\underline{V_{OUT}} \uparrow (More + )$ 

Negative Going Signal Base becomes less (+) WRT Emitter  $\rightarrow$  FB  $\uparrow \rightarrow$   $I_C \uparrow \rightarrow$  $V_{R_C} \uparrow \rightarrow$   $V_C \downarrow \rightarrow$  $V_{C_C} \downarrow \rightarrow$  $V_{OUT} \downarrow (Less +)$ 

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### **Common Collector Schematic**



### **Kirchoff Voltage Law**

DC Kirchoff Voltage Law Equations and Paths



 $\frac{\text{Base - Emitter Circuit}}{I_B R_B + V_{BE} + I_E R_E - V_{CC} = 0}$ 

 $\frac{\text{Collector} - \text{Emitter Circuit}}{I_C R_C + V_{CE} + I_E R_E - V_{CC} = 0}$ 

# **Common Collector Operation**



#### **Positive Going Signal**

Base becomes more (+) WRT Emitter  $\Rightarrow$  FB  $\uparrow \Rightarrow$   $I_E \uparrow \Rightarrow$  $V_{R_E} \uparrow \Rightarrow$   $V_E \uparrow \Rightarrow$  $\underline{V}_{OUT} \uparrow (More + )$ 

Negative Going Signal Base becomes less (+) WRT Emitter  $\rightarrow$  FB  $\downarrow \rightarrow$   $I_E \downarrow \rightarrow$  $V_{R_E} \downarrow \rightarrow$   $V_E \downarrow \rightarrow$  $V_{R_E} \downarrow \rightarrow$   $V_E \downarrow \rightarrow$ 

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### **Types of Bias Stabilization**

•Self Bias: A portion of the output is fed back to the input 180° out of phase. This negative feedback will reduce overall amplifier gain.

•*Fixed Bias:* Uses resistor in parallel with Transistor emitterbase junction.

•Combination Bias: This form of bias stabilization uses a combination of the emitter resistor form and a voltage divider. It is designed to compensate for both temperature effects as well as minor fluctuations in supply (bias) voltage.

•*Emitter Resister Bias:* As temperature increases, current flow will increase. This will result in an increased voltage drop across the emitter resistor which opposes the potential on the emitter of the transistor.

#### **Self Bias Schematic**



#### **Emitter Bias Schematic**



#### **Combination Bias Schematic**



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### **Class 'AB' Amplifier Curve**

#### Can be used for guitar distortion.



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### **Amplifier Coupling Methods**

•Direct: The output of the first stage is directly connected to the input of the second stage. Best Frequency Response -No frequency sensitive components.

•Impedance (LC) Coupling: Similar to RC coupling but an inductor is used in place of the resistor. Not normally used in Audio Amplifiers.

•*RC Coupling:* Most common form of coupling used. Poor Frequency Response.

•*Transformer Coupling*: Most expensive form coupling used. Mainly used as the last stage or power output stage of a string of amplifiers. 28 CENT-112 Fundamentals of Electricity and Electronics

#### **Direct Coupling Schematic**



### **RC Coupling Schematic**



### **Impedance Coupling Schematic**

