Question Bank of Digital Electronics

(BTES301-18)

1. Define gate.
2. Draw truth table of all logic gates.
3. Realize an AND, OR, NOT gate using NOR gates only.
4. Difference between multiplexer and demultiplexer.
5. What is a register? List various methods of loading data into shift register.
6. Difference between ROM & RAM.
7. How race around condition is eliminated in Master-slave J-K flip-flop?
8. Perform the following binary subtraction 01010101-11010101.
9. Convert following binary number into gray code & vice-versa: 10101111
10. Define multiplexer and demultiplexer.
11. Difference between accuracy and resolution for A/D converters.
12. Compare level triggering & edge triggering
13. Justify need of bus technology.
14. What are the functions of counters?
15. Difference between counter and register.
16. Define propagation delay.
17. Which device changes the parallel data into serial?
18. List various A/D& D/A conversion techniques
19. How many number of flip flops are required for a 7 Mod counter?
20. Define Maxterm & Minterm.
21. Add following numbers in 8-bit register using signed 2's complement notation: (i) 50 and -10 (ii) 55 and -75
22. What is the need for 1's complement and 2's complement arithmetic?
23. Compare PAL &PLA.
24. What is the significance of line termination?
25. Compare synchronous & asynchronous circuits.
26. Discuss the source of error in A/D conversion.

27. Define BCD Adder.
28. What is the function of D/A & A/D converters?
29. What do you mean by PLD's?
30. What is priority encoder?
31. Write first four decimal digits in base 6.
32. What is role of select lines in multiplexer?
33. What is a Universal register? Explain.
34. Describe the operations performed by an encoder and decoder ?
35. What is Cache Memory?
36. What are characteristics of memories?
37. What is the role of Shift-Registers?
38. Give the logic diagram and characteristics table of a clocked RS flip-flop.
39. What is race around condition? How it can be avoided?
40. Realize a half adder ckt using 4:1 MUX.
41. Design divide by 16 up-down counter.
42. Minimize the following using K-map

$$F(w,x,y,z)=\Sigma m(1,3,5,8,9,11,15) + d(2,13).$$

43. Compare the features of RAM,ROM,EEPROM,PLA,PAL
44. Describe internal architecture of PLDs.
45. Discuss with an example an design problem related to FPGA.
46. Design a decade counter..
47. Design a JK counter that goes threw states 2,4,5,7,2,4……
48. Write short note on transmission line effects.
49. Describe the advantage of using PLA over ROM for realizing Some Boolean functions.
50. Explain any one ADC technique you know.
51. Design syn BCD counter using JK flip-flop.
52. Give the structure of dedicated and shared bus.
53. Draw the diagram of JK,SR,D,T flip-flops and their truth tables.
54. Design a four bit parity checker ckt using (i) Gates and (ii) Mux.