Question Bank

Subject: Digital System Design

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Semester: 3rd

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Unit 1: Boolean Algebra & Combinational Circuits:

Logic gates; Boolean algebra; De Morgan's theorem, SOP & POS forms, canonical forms, Karnaugh maps up to 6 variables, binary codes, code Conversion, MSI devices like comparators; multiplexers; encoder; decoder; driver & multiplexed display; half and full adders; subtractors; serial and parallel adders; BCD adder; barrel shifter and ALU.

2 Marks Questions (Short Answer)

1. Convert as given:

   $(110001)_2$ = ( )$_{10}$

   $(65.535)_{10}$ = ( )$_{16}$

   Express $(10010011)_{BCD}$ and $(01100111)_{BCD}$ to binary and ex-cess-3 code.

   $(6CD.A)_{16}$ =( )$_{10}$

   $(BCA3.AD)_{16}$ = ( )$_2$

   Binary to gray (1001011) =( )$_{gray}$

   $(1776)_{10}$ = ( )$_2$

   Gray to binary (1001011) = ( )$_2$

   Multiply the terms $(1101 \text{ and } 101)_2$ and $(110110 \text{ and } 1100)_2$

   Subtract the terms $(1110\text{-}10111)_2$ and $(11011\text{-}10111)_2$

   Divide the terms $(1100/011)_2$ and $(110101/1001)_2$

   Subtract (-36) from (-15) using 2's compliment

   Subtract (+21) from (-13) using 2's compliment

   Add $(7F)_{16}$ and $(BA)_{16}$

   Subtract $(5C)_{16}$ from $(3F)_{16}$

2. Convert $(3000.45)_{10}$ into its equivalent octal number.
3. Convert the decimal fraction $(0.122)_{10}$ to its equivalent hex no.

4. Add $(DDCC)_{16}$ and $(BBAA)_{16}$
5. What are logic gates? Give examples.
6. State De Morgan's theorems.
7. Differentiate between SOP and POS forms.
8. Define canonical form.
9. What is a K-map? Why is it used?
10. What is the difference between binary and BCD?
11. Define a multiplexer and its use.
12. What is the function of an encoder?
13. Write the truth table of a half adder.
14. What is a barrel shifter?
15. Simplify ABC+AB.(AC)
16. Simplify AC (ABD) + ABCD + ABC
17. Convert the number 1011.101_2 to its decimal equivalent
18. Convert $(456)_{10}$ into binary
19. Convert $(42.9375)_{10}$ to binary
20. Convert $(25.012)_{10}$ into binary
21. convert $(49.21875)_{10}$ into octal
22. Convert $(472)_8$ into binary
23. convert $(10110001100)_2$ into octal
24. Convert the number $(356)_{16}$ to its decimal equivalent
25. Convert the number $(567.1875)_{10}$ to its Hexadecimal equivalent
26. Convert $(53)_{10}$ into Binary.

5 Marks Questions (Short Descriptive/Design-Based)

1. Simplify using Boolean algebra: A′B+AB′+ABA'B + AB' + ABA′B+AB′+AB
2. Obtain the simplified logical expression using K-maps:
   $Y= \sum m (1,5,7,9,11,13,15)$
   $Y=\sum m (1,2,9,10,11,14,15)$
3. Implement a 2-bit comparator using logic gates.

4. Simplify the following expressions once by considering the don't care condition and once by ignoring the don't care terms:
   $Y= \sum m (1,4,8,12,13,15) + d (3,14)$
   Also draw the logic circuit diagram for the same.
5. Simplify:
   $F(A\ B\ C\ D\ E) = \sum m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$
6. Minimize using K-Map:
   $Y=\Pi\ M(1,5,6,7,8,9,10,14)$
7. Design and explain full adder with the help of truth table and diagrams.
8. Design 8:1 Multiplexer for the given Expression: $Y=\sum m(0,1,2,4,6,8,10,12,14)$
9. Write a note on code converters with examples.
10. Design a 3-bit binary to Gray code converter.
11. Explain the working of a full subtractor with logic diagram.
12. Construct a 4:1 multiplexer and explain its operation.
13. Derive SOP and POS expressions for a 3-variable truth table.
14. Compare MSI devices: multiplexer, decoder, and driver.
15. Explain serial vs parallel adders.
16. Design a 2-bit BCD adder using full adders.
17. Reduce the following equation by using K-Map

    Y=ABC+ACD+AB+ABCD+ABC

10 Marks Questions (Long Descriptive/Design-Based)

18. Simplify the Boolean function using 4-variable K-map:
    $F(A,B,C,D)=\sum(0,1,2,5,6,7,8,9,10,14)$

    F(A,B,C,D) = (0,1,2,5,6,7,8,9,10,14)

    $F(A,B,C,D)=\sum(0,1,2,5,6,7,8,9,10,14)$
19. Design and explain a 4-bit binary subtractor using full adders.
20. Discuss the design and working of an ALU for 4-bit operations.
21. Explain different binary codes and their applications.
22. Design a 4-bit parallel adder circuit using logic gates.
23. Implement $F (A, B, C, D) = \sum (1,3,7,11,15)$ using K-map and derive simplified expression.
24. Design a 2-bit comparator circuit.
25. Explain the construction and working of a 4x1 multiplexer using basic gates.

26. Write a detailed note on decoder-driver circuits and display interfacing.
27. Compare SOP and POS in terms of implementation and efficiency.
28. Simplify and implement using K-Map technique. Also realize the expression. f(ABCD)= Σm(1,3,4,6,9,10,11,12,14,15)

Unit 2: Sequential Circuits:

Building blocks of sequential circuits like S-R, J-K,T & D flip-flops; master-slave J-K FF; edge triggered FF; ripple counters; synchronous counters; shift registers; finite state machines; design of synchronous FSM, algorithmic state machines charts; designing synchronous circuits like pulse train generator; pseudo random binary sequence generator; clock generation.

2 Marks Questions

1. Explain the race condition
2. What do you mean by buffer?
3. Define S-R flip-flop with symbol.
4. What is edge triggering?
5. What is the main advantage of JK flip-flop over SR flip-flop?
6. Define synchronous counter.
7. What is a ripple counter?
8. Explain the working of a ripple counter with the timing diagram and also show how it counts?
9. Convert SR Flip Flop into JK Flip Flop.
10. Differentiate Synchronous and Asynchronous Sequential Circuits.
11. Draw the truth table of D flip-flop.
12. What is the use of a shift register?
13. Define finite state machine (FSM).
14. What is the difference between Mealy and Moore machines?
15. What is the use of a pseudo random binary sequence generator?
16. What is the difference between level and edge triggering? Explain the working of master slave JK flip flop.
17. Design a synchronous decade counter o count the following sequence:

    1, 0, 2, 3, 4, 8, 7, 6, 5

18. What is the basic difference between a counter and a shift register?
19. What is the meaning of lock out in counters?
20. Design a BCD counter using JK flip flop

5 Marks Questions

1. Explain the working of an edge-triggered JK flip-flop.
2. Design a 3-bit asynchronous counter.
3. Explain the function of a universal shift register.
4. Draw the block diagram and explain a pulse train generator.
5. Design a synchronous 3-bit up counter.
6. Write a note on algorithmic state machine (ASM) chart.
7. Design gray to excess-3 code converter using NAND gate
8. Design a MOD-30 synchronous UP counter
9. Design MOD-16 up-down counter
10. What do you mean by self starting counter?
11. Explain the operation of a T flip-flop.
12. Differentiate between synchronous and ripple counters.
13. Describe the structure of a master-slave flip-flop.
14. Draw and explain a simple FSM diagram for detecting the pattern “101”.

10 Marks Questions

1. Design and explain a sequence detector for the sequence “1101” using FSM.
2. Explain the design and operation of a 4-bit shift register.
3. Describe the working and application of a pseudo random binary sequence generator.
4. Draw and explain the ASM chart for a 3-state system.
5. Design a 3-bit synchronous counter using JK flip-flops.
6. Explain with diagrams the operation of ripple and synchronous counters.
7. Design and explain a circuit for clock pulse generation using flip-flops.
8. Explain the design of a Moore FSM with an example.
9. Explain the difference between various flip-flops with truth tables.
10. Discuss shift registers and their applications in digital systems.

11. Design a MOD-10 Gray code decade counter sequence by using RS flip flop

    0,1,3,2,6,14,10,11,9,8

12. Design a mod 10 up down counter by using JK flip flop.
13. Design the counter circuit from the given state diagram using JK and T flip flops.

Unit 3: Programmable Devices & ADC/DAC

Specifications: noise margin, propagation delay, fan-in, fan-out, Tristate; TTL, ECL, CMOS families and their interfacing; architectures of PLA, PAL, GAL, CPLD&FPGA. DAC: weighted resistor, R-2R ladder, resistor string; ADC: single slope, dual slope, successive approximation, flash.

2 Marks Questions

1. Define noise margin.
2. What is propagation delay?
3. What is fan-out in digital circuits?
4. What do you mean by PALs?
5. Write any two differences between TTL and CMOS.
6. What is a tri-state buffer?
7. Give two applications of FPGA.
8. What is a DAC?
9. What is the role of a sample-and-hold circuit in ADC?
10. Define successive approximation ADC.
11. Name any two programmable logic devices.

5 Marks Questions

1. Differentiate between TTL and ECL logic families.
2. Explain the architecture of a PAL device.
3. Describe the working of R-2R ladder DAC.
4. Compare weighted resistor DAC and resistor string DAC.
5. Explain the working of a flash ADC with a block diagram.
6. Write a short note on CPLD and FPGA.
7. Explain interfacing between TTL and CMOS families.

8. Describe the working of a dual slope ADC.
9. List and explain parameters affecting logic family selection.
10. Explain the architecture and working of a PLA.
11. Explain the operation and principle of successive approximation A/D converter.
12. Define the term quantization error?
13. What is the advantage of R-2R ladder DAC over weighted resistor DAC?
14. Explain R-2R ladder digital to analog converter with the help if suitable circuit diagram?
15. Explain the architecture and function of programmable logic arrays?
16. Briefly explain the characteristics of memories.
17. Explain Resistor- Transistor logic?
18. Explain Diode-Transistor logic?
19. Explain Transistor-Transistor logic?
20. Explain Emitter coupled logic?
21. Explain Direct- coupled transistor logic?
22. What are IC's? Explain its characteristics?
23. Compare the various logic families.
24. Define the term current hogging in DCTL.
25. How is high speed operation is possible in ECL gates?
26. Which family has higher noise margin ECL or TTL? and Why?

10 Marks Questions

1. Compare different logic families: TTL, ECL, CMOS in terms of speed, power and compatibility.
2. Explain in detail the working of successive approximation ADC.
3. Draw and explain the architecture of CPLD and FPGA.
4. Describe and compare different DACs (Weighted Resistor, R-2R Ladder, Resistor String).
5. Explain various types of ADCs and their applications.
6. Draw and explain a complete ADC system with signal conditioning.
7. Discuss interfacing of TTL and CMOS devices with practical considerations.

8. Explain tristate logic with truth table and practical applications.
9. Design a DAC using R-2R ladder and calculate output for a 4-bit input.
10. Write a comparative analysis of PLA, PAL, GAL and CPLD.

Unit 4: Introduction to VHDL

VHDL constructs; Data types and objects; different modelling styles in VHDL; Dataflow, Behavioural and Structural Modelling; Synthesis and Simulation; HDL programming for basic combinational and sequential circuits.

2 Marks Questions

1. What does VHDL stand for?
2. Describe different types of data in VHDL.
3. Define ‘signal’ and ‘variable’ in VHDL.
4. What is a port map?
5. What are the modeling styles in VHDL?
6. Write the syntax of an entity declaration in VHDL.
7. What is dataflow modeling?
8. Mention any two data types in VHDL.
9. Define synthesis.
10. What do you mean by Finite state machines.
11. What is the use of structural modeling?
12. What is the difference between simulation and synthesis?

5 Marks Questions

1. Write a VHDL code for a 2:1 multiplexer using dataflow modeling.
2. Differentiate between dataflow, structural and behavioral modeling.
3. Explain the basic constructs used in VHDL.
4. Write a behavioral VHDL code for a D flip-flop.
5. Explain the importance of simulation in VHDL.
6. Design a 2-input AND gate using structural modeling in VHDL.
7. Explain any 3 predefined data types in VHDL with examples.
8. Write a VHDL code for 4-bit binary counter.

9. Write the VHDL code for a half adder using dataflow modeling.
10. Explain the concept of process block in behavioral modeling.
11. Explain different modelling styles in VHDL. Write about behavioural and structural modelling

10 Marks Questions

1. Write and explain a VHDL code for a 4:1 multiplexer using all three modeling styles.
2. Design and implement a 4-bit ripple counter using VHDL.
3. Write a behavioral VHDL code for a 3-bit sequence detector.
4. Discuss the synthesis process and how it differs from simulation.
5. Write and explain the VHDL code for a full adder using structural modeling.
6. Explain how VHDL can be used to design a shift register.
7. Describe the use of testbenches in verifying VHDL code.
8. Write a VHDL program to implement a 2-bit comparator.
9. Compare various modeling styles in VHDL with examples.
10. Discuss the complete VHDL design flow from design entry to simulation.